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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/662,900

09/15/2003

Cyril Cabral JR.

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08/22/2005

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EXAMINER

PHAM, LONG

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/662,900		CABRAL ET AL.	
	Examiner		Art Unit	
	Long Pham		2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

New grounds of rejection

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicants' admitted prior art (AAPA) of this application in combination with Maex et al. (US publication 2002/0151170) and Van Kestersen et al. (US patent 5,952,094).

3. With respect to claims 1 and 17, AAPA teaches a method of fabricating a silicide on the surface of a SiGe containing substrate comprising the steps of (see figs. 1A-1C, 2A-2B, and 3A-3E, and the Background of Invention on pages 1, 2, and part on page 3 of this application):

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providing a structure including a Co layer on top of a SiGe containing substrate;

subjecting the structure to a silicide process so as to form a solid solution of cobalt disilicide.

AAPA fails to teach adding Ni to the Co layer.

Maex et al. teach including Ni to a Co layer before siliciding process. See the abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to add Ni to the Co layer of AAPA to accelerate the formation of disilicide phase. See [0085].

Also with respect to claim 1, Maex et al. teach self-aligned silicide process. See [0077].

Also with respect to claims 1 and 17, Since AAPA in combination with Maex et al. teach the claimed process, a solid solution of Co and Ni containing disilicide would inherently form and the Ni would inherently reduce the formation temperature of the disilicide.

With respect to claims 2 and 17, Maex et al. further teach that a first anneal done at a first temperature of 550 degrees Celsius that is inherently capable of forming a high resistance silicide phase material, a selective etch to remove unrelated metal from regions not in contact with the substrate, and a second anneal done at a second temperature that is higher than the first temperature of the first anneal. See the abstract, [0054] to [0090].

With respect to claim 3, Maex et al. further teach the first anneal is done at 550 degrees Celsius for a time period of 30 seconds. See [0054].

With respect to claim 4, Maex et al. further teach the second anneal is done at 700 degrees Celsius for a time period of 30 seconds. See [0054].

With respect to claims 5, 6, and 10, Maex et al. further teach the Co layer comprises at least 25 percent of Ni. See claim 12.

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With respect to claim 7, Maex et al. further teach that the Co layer is a Co-Ni alloy. See [0014] and claim 12.

With respect to claims 8 and 9, Maex et al. appear to fail to teach adding Re to the layer or alloy layer for forming disilicide.

Van Kesteren et al. teach adding Re to a Co layer to reduce Curie temperature and magnetization. See the abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to add RE to the alloy or Co layer of AAPA to obtain the above advantage.

With respect to claim 11, Maex et al. further teach the first and second anneals comprises a rapid thermal annealing process. See [0054].

With respect to claim 12, the heating in presence of nitrogen to form silicide is well-known.

With respect to claim 13, AAPA and Maex et al. appear to fail to teach the range for the annealing temperature rate.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the annealing temperature rate through routine experimentation and optimization to obtain optimal or desired device performance because the annealing temperature rate is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claims 14 and 15, Maex et al. further teach a diffusion barrier of Ti is formed atop the Co layer comprising at least Ni. See [0055] and [0077].

With respect to claim 16, Maex et al. further teach the diffusion barrier is removed by the selective etching step of the self-aligned silicide process. See [0055] and [0077].

Response to Arguments

4. Applicant's arguments with respect to claims 1-17 have been considered but are moot in view of the new ground(s) of rejection.

In response to the applicant's arguments in the paragraph connecting pages 8 and 9 of the amendment dated 06/07/05, it is submitted since AAPA in combination of Maex et al. teach adding Ni to the co layer before siliciding process as presently claimed, the presence of Ni would inherently reduce formation temperature of the disilicide. Further, it is submitted that where claimed and prior art products are identical or substantially identical in structure or composition (material) or are produced by identical or substantially identical processes, claimed function or properties are presumed to be inherent. In re Best, 195 USPQ 430, 433 (CCPA 1977).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP